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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ART UNIT	PAPER NUMBER
2644	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/751,417	ANDERSON ET AL.
	Examiner	Art Unit
	Walter F Briney III	2644

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

Claims 1-3, 8-10, 15, 16, 19-21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson et al. (US Patent 6,477,249) in view of Hendricks et al. (US Patent 6,625,278) and further in view of Frantz et al. (US Patent 5,802,169).

Claim 19 is limited to **an apparatus supporting transmission of signals carrying voice and data on a subscriber line, comprising: a subscriber line interface circuit adapted to receive an input signal having a voice, data, and DC component**; Williamson discloses a POTS line card (figure 1, element 11) and POTS xDSL splitter (figure 1, element 15) that receive voice, data, and DC signals from a telephone line (i.e. input signal) (figure 1, element 20), which make up a subscriber line interface circuit. Claim 19 is further limited to **a first filter adapted to filter at least a portion of the data component of the input signal to provide a filtered data signal**; Williamson discloses a LPF (figure 3) as part of the splitter (figure 1, element 15) for removing data components from a telephone line input signal destined for a POTS line card. Williamson discloses the difficulty of terminating the telephone line with a POTS/xDSL splitter because of impedance mismatch, but solves it by using different filters for different situations (column 2, line 66-column 3, line 15). Therefore, Williamson has been shown to disclose all limitations of the claim with the exception **wherein the subscriber line interface circuit includes a first loop adapted to adjust an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal**; Hendricks teaches to use an impedance

matching filter to match the terminating impedance of a subscriber line card to that of the impedance of the loop it is connected, where the filter provides flexibility for different standards that switchable networks, like that of Williamson, do not (column 1, lines 35-48). Hendricks' filter includes a first loop consisting of a reference impedance (figure 1, element 170) that corresponds to a maximum AC impedance (i.e. input impedance/preselected value/voice band) (column 4, lines 4-18). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the impedance matching filter of Hendricks with a first loop for the purpose of matching the terminating impedance of the subscriber line card of Williamson to the impedance of the subscriber line with increased flexibility over the switchable filter arrangement of Williamson. Claim 19 is further limited to **a digital signal processor**; Hendricks teaches a digital signal processor (figure 1, element 195) for use in the impedance matching filter. The digital signal processor **comprising: a second feedback loop adapted to adjust the input impedance of the apparatus from the first preselected value to a second preselected value**; Hendricks teaches a second loop with a digitally controlled current source (figure 1, element 160) that drives current in parallel to the reference impedance, therefore changing the input impedance, where the current supplied is varied throughout a desired range (i.e. second preselected value) (column 2, lines 19-40). The digital signal processor also comprising **a third feedback loop adapted to adjust at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value**; Hendricks teaches a third loop with a digital filter (figure 1, element 110) that adjusts the gain (i.e. magnitude) of a received

signal (i.e. filtered signal) and further controls the current output by the current source (figure 1, element 160). If the signal or state of the line changes the impedance is varied to a new value (i.e. change impedance to a third value) (column 2-column 5). Therefore, Williamson in view of Hendricks has been shown to make obvious all the limitations of the claim with the exception of **a second filter adapted to filter at least a portion of the DC component of the filtered data signal to provide a filtered signal**; Hendricks teaches operating on AC signals and preferably avoiding DC signals (Hendricks, column 3, lines 27-28). Frantz teaches removing DC signals from AC impedance matching circuitry using a capacitor in series with a transformer (i.e. second filter) with its primary winding connected across the tip and ring line forming a loop (column 3, lines 55-63 and figure 1, elements 113 and 115). It would have been obvious to one of ordinary skill in the art at the time of the invention to block DC signals from the impedance matching circuitry as taught by Frantz for the purpose of performing impedance matching only on AC signals input to the subscriber line interface circuit of Williamson in view of Hendricks.

Claims 1, 8, 15, and 24 are essentially the same as claim 19 and are rejected for the same reasons.

Claim 20 is limited to **the apparatus of claim 19**, as covered by Williamson in view of Hendricks and further in view of Frantz, **wherein the subscriber line integrated circuit is a voltage subscriber line interface circuit**; Williamson discloses a POTS line card where one purpose of a line card at a central office is to supply

voltage to a subscriber line. Therefore, Williamson in view of Hendricks and further in view of Frantz makes obvious all the limitations of the claim.

Claim 21 is limited to **the apparatus of claim 19**, as covered by Williamson in view of Hendricks and further in view of Frantz, **wherein the feedback loop comprises: a filter capable of removing at least a portion of a residual DC component from the filtered signal and providing an output signal**; Hendricks teaches a digital filter whose transfer function is set to reject DC (column 5, lines 31-41). Claim 21 is further limited to **a Z-filter block capable of adjusting at least one of a gain and phase of the output signal**; Hendricks teaches that the filter adjusts the gain of the output signal (column 4, lines 59-64). Therefore, Williamson in view of Hendricks and further in view of Frantz makes obvious all the limitations of the claim.

Claim 16 is essentially the same as claim 21 and is rejected for the same reason.

Claim 9 is limited to **the apparatus of claim 8**, as covered by Williamson in view of Hendricks and further in view of Frantz, **wherein the second filter includes a DC cancellation loop capable of removing the portion of the DC component**; Frantz teaches removing a DC component from an AC impedance matching circuit by placing a capacitor in series with an AC coupling transformer between the tip and ring lines creating a loop (column 3, lines 55-63 and figure 1, elements 113, 114, and 14). Therefore, Williamson in view of Hendricks and further in view of Frantz makes obvious all limitations of the claim.

Claim 2 is essentially the same as claim 9 and is rejected for the same reasons.

Claim 10 is limited to **the apparatus of claim 8**, as covered by Williamson in view of Hendricks and further in view of Frantz, **wherein the first filter comprises a single-pole low pass filter**; Williamson discloses a low pass filter (i.e. first filter) with a single pole corresponding to an inductor in series with one of the twisted pair lines (figure 8) that is used to block data signals. Therefore, Williamson in view of Hendricks and further in view of Frantz makes obvious all limitations of the claim.

Claim 3 is essentially the same as claim 10 and is rejected for the same reasons.

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson in view of Hendricks in view of Frantz as applied to claim 19 above, and further in view of Martin (US Patent 4,577,255).

Claim 22 is limited to **the apparatus of claim 21**, as covered by Williamson in view of Hendricks and further in view of Frantz, **further including at least one resister for defining the input impedance of the apparatus to a selected value for the data band**; Martin teaches providing an impedance termination match (i.e. input impedance) between a DSL loop (i.e. data band/selected value) and a DSL transceiver (i.e. apparatus) using a network including a resistor (figures 1 and 2, element 11) (column 1, line 63-column 2, line 10). It would have been obvious to one of ordinary skill in the art to provide the resistive network as taught by Martin for the purpose of matching the DSL terminating impedance of the DSL transceiver and subscriber loop of Williamson.

Claim 23 is limited to **the apparatus of claim 22**, as covered by Williamson in view of Hendricks in view of Frantz and further in view of Martin, **wherein the selected value is in a range of 100 to 135 ohms**; Martin teaches providing DSL termination

impedance (i.e. selected value) of 100 ohms (column 1, line 63-column 2, line 10). Therefore, Williamson in view of Hendricks in view of Frantz and further in view of Martin makes obvious all limitations of the claim.

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson in view of Hendricks in view of Frantz as applied to claim 1 above, and further in view of Martin.

Claim 4 is essentially the same as claim 22 and is rejected for the same reasons.

Claim 5 is essentially the same as claim 23 and is rejected for the same reasons.

Claim 6 is limited to **the method of claim 4**, as covered by Williamson in view of Hendricks in view of Frantz and further in view of Martin, **wherein adjusting the input impedance includes adjusting the frequency characteristic of the filtered signal by a selected interval**; Hendricks teaches filtering a received signal (i.e. adjusting the frequency characteristic by a selected interval) and using the output voltage of the filtered signal to control the output of the current source, which directly controls the input impedance. Therefore, Williamson in view of Hendricks in view of Frantz and further in view of Martin makes obvious all limitations of the claim.

Claim 7 is limited to **the method of claim 4**, as covered by Williamson in view of Hendricks in view of Frantz and further in view of Martin, **wherein the first preselected value is in a range of 600 to 1200 ohms**; Hendricks teaches using a reference impedance to set the maximum value of input impedance that will be needed (column 4, lines 4-18) and that the maximum of the range of impedances needed is 1050 ohms

(column 2, lines 19-24). Therefore, Williamson in view of Hendricks in view of Frantz and further in view of Martin makes obvious all limitations of the claim.

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson in view of Hendricks in view of Frantz as applied to claim 8 above, and further in view of Martin.

Claim 11 is essentially the same as claim 22 and is rejected for the same reasons.

Claim 12 is essentially the same as claim 23 and is rejected for the same reasons.

Claim 13 is limited to **the apparatus of claim 12**, as covered by Williamson in view of Hendricks in view of Frantz and further in view of Martin, **wherein the second impedance block and the third impedance block comprise a programmable impedance matching filter**; Hendricks teaches matching impedance using a voltage controlled current source (i.e. second impedance block) (figure 1, element 160) and a digital filter (i.e. third impedance block) (figure 1, element 195) where the digital filter controls (i.e. programs) the current source (column 2, lines 12-40). Therefore, Williamson in view of Hendricks in view of Frantz and further in view of Martin makes obvious all limitations of the claim.

Claim 14 is limited to **the apparatus of claim 12**, as covered by Williamson in view of Hendricks in view of Frantz and further in view of Martin, **wherein the first impedance block adapted to adjust the input impedance includes the first impedance block adapted to adjust the frequency of the filtered signal**; Hendricks

discloses a reference impedance (i.e. first impedance block) (figure 1, element 170) that further adjusts the signal characteristics (i.e. adjust the frequency) of the DC blocked signal (i.e. filtered signal) (column 4, lines 4-18). Therefore, Williamson in view of Hendricks in view of Frantz and further in view of Martin makes obvious all limitations of the claim.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williamson in view of Hendricks in view of Frantz as applied to claim 15 above, and further in view of Martin.

Claim 17 is essentially the same as claim 22 and is rejected for the same reasons.

Claim 18 is essentially the same as claim 23 and is rejected for the same reasons.

Response to Arguments

Applicant's arguments with respect to claims 1-24, filed 3 March 2004, have been fully considered but they are not persuasive.

With respect to claim 19, the applicant alleges that the prior art references do not teach that the AC signal is the same as **the filtered data signal** (amendment, filed 3 March 2004, page 11, second paragraph); the examiner respectfully disagrees. In particular, Williamson discloses a POTS line card (Williamson, figure 1, element 11) that is situated behind a POTS/xDSL splitter (Williamson, figure 1, element 15). Thus, the input signal to the POTS line card is **a filtered data signal**. Since there is no distinction

to what components the signal is meant to comprise after filtering, the examiner assumes **the filtered data signal** is a POTS + DC signal (i.e. AC + DC signal).

Now that the input to the line card is clearly distinguished, attention is turned to how the remaining input is filtered. The teaching of Hendricks supplies the technical background to adaptively adjust a line card's impedance for superior performance. Notice, the impedance matching (Hendricks, figure 1, element 100) is performed directly in front of a line card (Hendricks, figure 1, element 150), which means its input is the same as the line card's. Furthermore, only AC impedances are matched, while DC resistance is ignored (Hendricks, column 3, lines 27-28). However, Hendricks is not relied upon for a description of how to remove DC components such that they are not used in termination impedance calculations. Frantz is relied upon to teach that voice frequency line card inputs can be coupled with a capacitor and transformer (Frantz, column 3, lines 55-63) (Frantz, figure 1, elements 115, 114).

With respect to the above, the prior art teaches all claimed limitations. The desirability to motivate has also been pointed out (i.e. the teaching of matching AC impedances). Success is clear in view of the validity of both the Hendricks and Frantz teachings.

Therefore, the arguments for claim 19 are not persuasive. It follows that the arguments for claims 1-18 and 20-24 are essentially the same and are not persuasive for the same reasons.

Because the arguments have been found to be not persuasive, the examiner has represented the rejections exactly as they appeared in the previous office action, filed 2 December 2003.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER